Am27S41/27PS41

16,384-Bit (4,096 x 4) Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- Ultra-fast access time "A" version (35 ns Max.) — Fast access time Standard version (50 ns Max.) — allow
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm

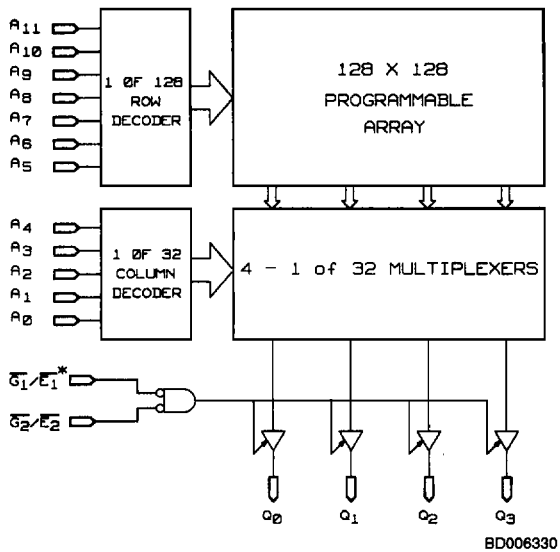
GENERAL DESCRIPTION

The Am27S41 (4,096-words by 4-bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy-word depth expansion is facilitated by active LOW ($\overline{G_1}$ & $\overline{G_2}$) output enables.

This device is also offered in a power-switched version, the Am27PS41.

BLOCK DIAGRAM



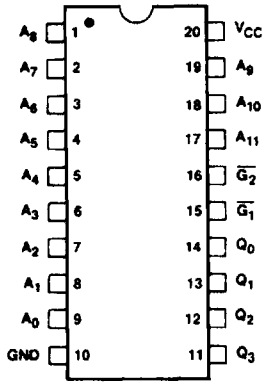
*E nomenclature applies only to Am27PS power-switched versions.

PRODUCT SELECTOR GUIDE

Part Number	27S41A		27S41		27PS41	
Address Access Time	35 ns	50 ns	50 ns	65 ns	50 ns	65 ns
Operating Range	C	M	C	M	C	M

Publication # 02122 | Rev. C | Amendment /0
Issue Date: May 1986

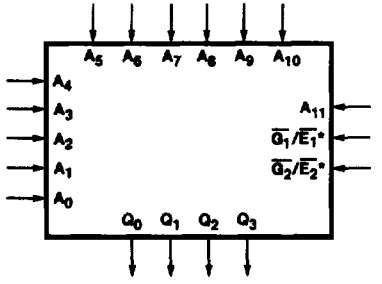
CONNECTION DIAGRAMS
Top View



CD000411

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



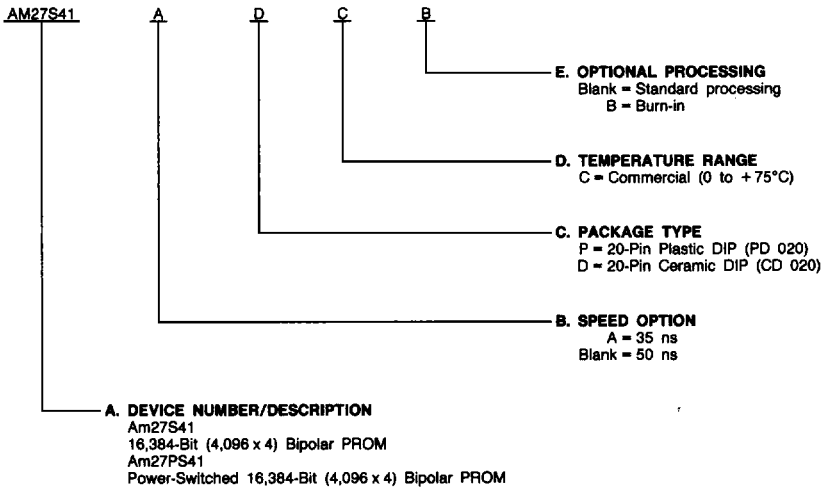
LS000041

*E nomenclature applies only to Am27PS power-switched versions.

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27S41	PC, PCB, DC, DCB
AM27S41A	
AM27PS41	

Valid Combinations

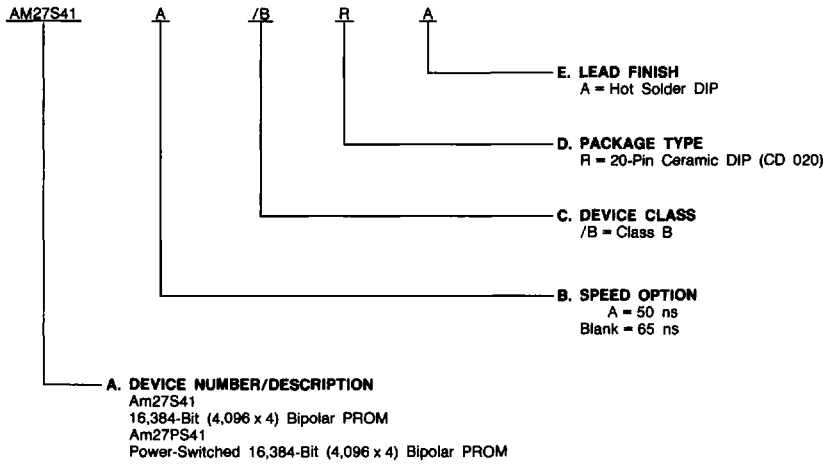
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**

B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S41	/BRA
AM27S41A	
AM27PS41	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{11}$ Address Inputs
The 12-bit field presented at the address inputs selects one of 4,096 memory locations to be read from.

$Q_0 - Q_3$ Data Output Port
The outputs whose state represents the data read from the selected memory locations.

$\overline{G_1}$, $\overline{G_2}$ Output Enable
Provides direct control of the Q-output, three-state buffers. Outputs disabled forces all outputs to a floating or high-impedance state. On power-switched version, the disabled state reduces the I_{CC} to I_{CCD}.

$$\text{Enable} = \overline{G_1} \cdot \overline{G_2}$$

$$\text{Disable} = \overline{\overline{G_1} \cdot \overline{G_2}}$$

$$= G_1 \cdot G_2$$

V_{CC} Device Power Supply Pin
The most posi' ve of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

FUNCTIONAL DESCRIPTION

Power Switching

The Am27PS41 is a power-switched device. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, I_{CC} is reduced to half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS41 is selected by a low level on $\overline{E_1}$, a current surge is placed on the V_{CC} supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1 μf ceramic capacitor be connected from pin 20 to pin 10 at each device. (See Figure 1.)

2. Address access time (TAVQ1) can be optimized if a chip enable set-up time (TEVAV) of greater than 25 ns is observed. Negative set-up times on chip enable (TEVAV < 0) should be avoided. (For typical and worse case characteristics, see Figures 2A and 2B.)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to + 5.5 V
DC Input Current ..... −30 mA to +5 mA

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Military Products 100% tested at case temperature −55°C, +25°C, 125°C

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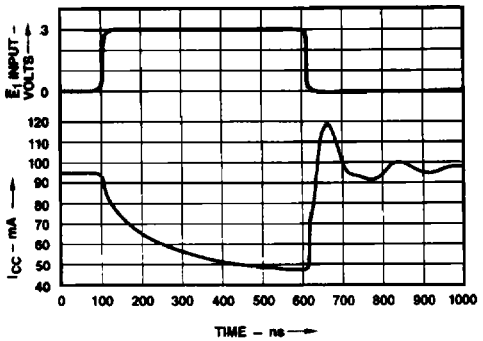
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}	COM'L			0.45	Volts
			MIL			0.50	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}				40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 1)	COM'L	−20		−90	mA
			MIL	−15		−90	
I_{CC}	Power Supply Current	V_{CC} = Max. All inputs = 0.0 V	COM'L			165	mA
			MIL			170	
I_{CCD}	Am27PS Version Power Down Supply Current	V_{CC} = Max. V_{E_1} = 2.4 V, All other inputs = 0.0 V				85	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. $V_{\overline{G_1}}$ = 2.4 V	V_O = V_{CC}			40	μA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 2)			5.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 2)			8.0		

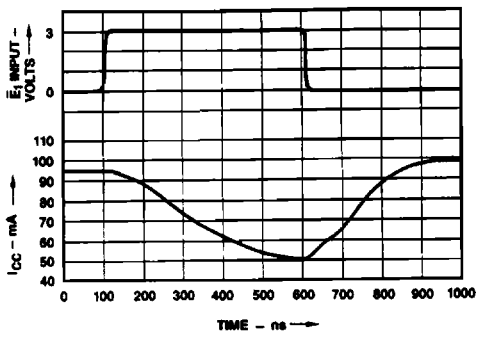
Notes: 1. Not more than one output should be shorted at a time. Duration of the short circuit test should not be more than one second.
2. These parameters are not 100% tested, but are periodically sampled.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

*See the last page of this spec for Group A Subgroup Testing information.

TYPICAL DC and AC OPERATING CHARACTERISTICS



Typical I_{CC} Current Surge without 0.1 mF (I_{CC} is Current Supplied by V_{CC} Power Supply)



Typical I_{CC} Current Surge with 0.1 mF (I_{CC} is Current Supplied by V_{CC} Power Supply)

Figure 1. I_{CC} Current

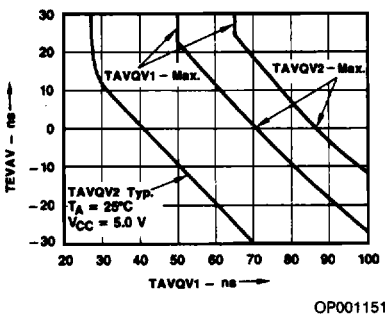


Figure 2A. TAVQV1 versus TEVAV

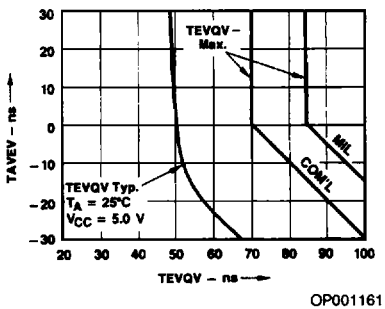
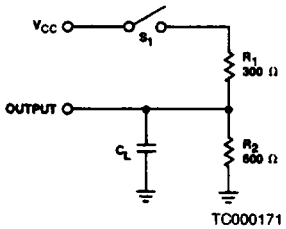


Figure 2B. TEVQV versus TAVEV

SWITCHING TEST CIRCUIT



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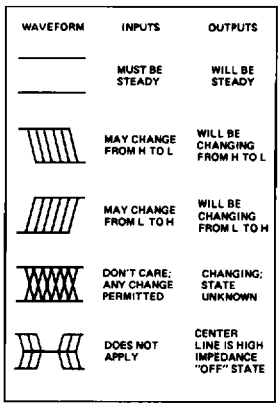
KEY TO SWITCHING WAVEFORMS



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SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

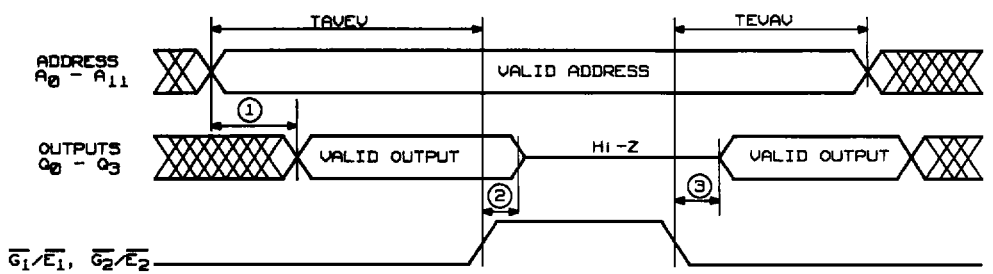
No.	Parameter Symbol	Parameter Description	Version	27S Version COM'L Min.	27S Version COM'L Max.	27S Version MIL Min.	27S Version MIL Max.	27PS Version COM'L Min.	27PS Version COM'L Max.	27PS Version MIL Min.	27PS Version MIL Max.	Units
1	TAVQV	Address Valid to Output Valid Access Time	A		35		50					ns
			STD		50		65		50		65	
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z	A		25		30					ns
			STD		25		30		25		30	
3	TGVQV	Delay from Output Enable Valid to Output Valid	A		25		30					ns
			STD		25		30		60		65	
4	TAVQV1	Power Switched Address Valid to Output Valid Access Time (Am27PS Versions only)	A						60		65	ns
			STD						80		90	

See Switching Test Circuit.

Notes: 1. TAVQV is tested with switch S_1 closed and $C_L = 5$ pF. TEVAV is defined as chip enable setup time.
2. For the three-state output, TGVQZ is tested with $C_L = 5$ pF to the 1.5 V level; S_1 is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. TGVQV is tested with $C_L = 5$ pF. HIGH to high-impedance tests are made with S_1 open to an output voltage of steady state HIGH −0.5 V; LOW to high-impedance tests are made with S_1 closed to the steady state LOW +0.5 V level.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



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GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVQV	9, 10, 11
2	TGVQZ	9, 10, 11
3	TGVQV	9, 10, 11
4	TAVQV1	9, 10, 11
	Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.